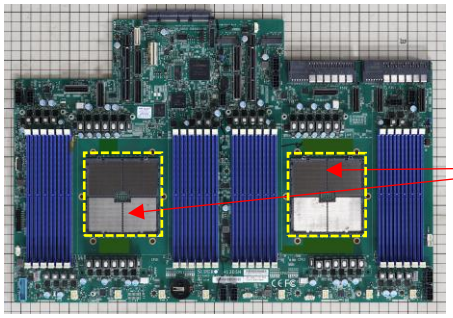
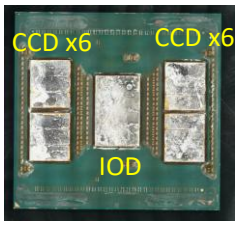
Server: AMD EPYC 9825-equipped Supermicro Server PCB and Package Analysis Report (Announcement)

Supermicro: 2U Hyper A+ Server (AS -2025HS-TNR)



Main PCB

Package



Package
After remove heat sink

Product Overview

The AMD EPYC 9825 is a 128-core CPU adopting a chiplet architecture, consisting of 12 Zen 4c CCDs and one I/O die. The CCDs are manufactured using a 5nm process, while the IOD is produced with a 6nm process, and they are interconnected via Infinity Fabric. With its high-density and high-efficiency design, it is optimized for cloud and HPC applications. Infinity Fabric is a high-speed interconnect technology developed by AMD to link both within and between chips. It plays a central role in integrating multiple chiplets to function as a single processor.

This time, LTEC is going to release the following five reports:

- Investigation of semiconductor components mounted on the PCB
- Cross-section analysis of the board and package
- L/W measurement of the finest features across 14 board layers
- Plane view image data of 20 package layers
- Analysis of CCD and IOD chips (Top layer, Gate layer, SEM cross-section [Seal Ring])

Details will be provided on the next page.

Note
CCD: Core Compute Die
IOD : I/O Die

Report No : 25R-0714-1,2,3,4,5 Release day :

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Report

1. Report (1) : Survey of Key Semiconductor and Components mounted on the PCB

Scheduled Release: November 30
- Survey of mounted semiconductor devices
- Datasheets (if available)
- Enlarged photographs of mounted components such as sockets

2. Report (2) : Cross-section Analysis of PCB and Package

Scheduled Release: November 30
- X-ray images of the package
- Cross-section structural analysis
- Measurement of individual layer thicknesses

3. Report (3) : L/W Measurement of the Finest Features Across each 14 PCB Layers

Scheduled Release: December 19
- Measurement of line width and line pitch of the finest features in each of the 14 layers

4. Report (4) : Image Data of 20 Package Layers

Scheduled Release: November 30
- Wiring information (photographs of each of the 20 layers, line width, line pitch)
- Optional: CAD data (ODB++ etc.) available (additional fee is required)

5. Report (5) : Analysis of CCD and IOD Dies

Scheduled Release: January 30, 2026
SEM cross-section of Seal Ring area
Photographs of top layer and gate layer
Optional: Functional estimation available (additional fee is required)

For inquiries regarding report pricing, please feel free to contact LTEC.

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