New Release

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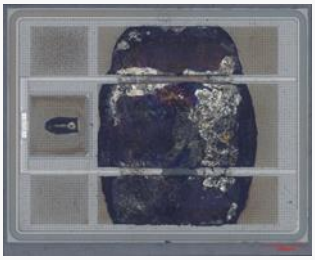
SiC MOSFET(1200V) : ON Semiconductor(equipped in Kia EV6 GT) Power card Structure, Process analysis Reports.

Kia EV6 GT (From web information)

(https://www.kia.com/uk/new-cars/ev6-gt/#text_441302445)

Power card appearance



SiC MOSFET die

Report summary

The Kia EV6 GT was announced by Kia Motors, a subordinate of Hyundai Motors, in March 2021, and is high-performance model of the company's first BEV (battery electric vehicle) Kia.
The inverter that drives the rear motor of EV6(2022model) consists of two units. One inverter is for normal mode using Infineon Si-IGBT module, another inverter is added during high output mode using ON Semiconductor (OnSemi) SiC power cards.
This time, LTEC released two reports (1. Structure analysis report and 2. Process analysis report) of OnSemi SiC MOSFET power card equipped in this inverter.

Product specifications/features

Product number : NVVR26A120M1WSS 1200V SiC MOSFET Power card

Product release date: 2022

Analysis Contents/Overview of Results

1. Structure analysis Report (98 pages)

- A two-layer metal process is used to maximize transistor area.
- Cu ribbon is used for the source wire, and Ag sinter is used for die attach.
- The power module uses a DBC substrate, and the insulation layer is Al, N based.

2. Process analysis Report (42 pages)

- The on-resistance per unit area (RONxA 465mΩ·mm^2) is equivalent to other companies' 2nd to 3rd generation SiC process.
- The thickness of the N-epi (drift) layer and doping concentration are extracted and correlated with the measured breakdown voltage BVdss.
- Estimating the manufacturing process flow and the number of photo/masking steps.

Please contact us for report pricing.

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Report No : 23G-0469-1,2
Release day: 2023.10.31

(1) Excerpt from structure analysis report

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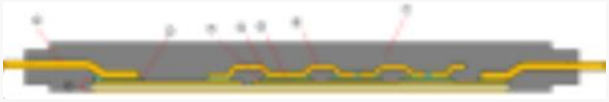
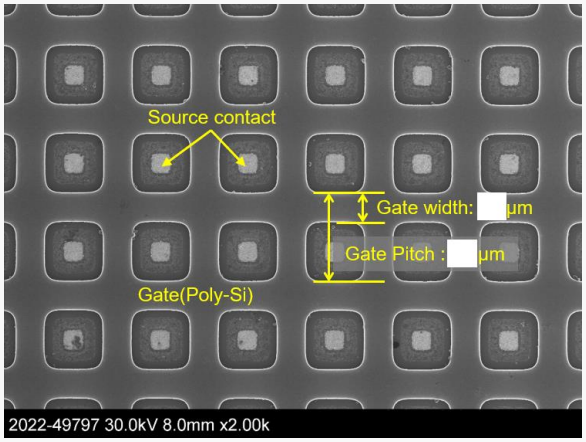
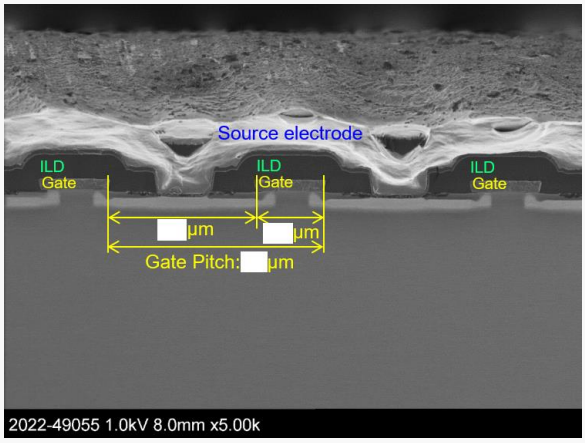
(1) Excerpt from structure analysis report



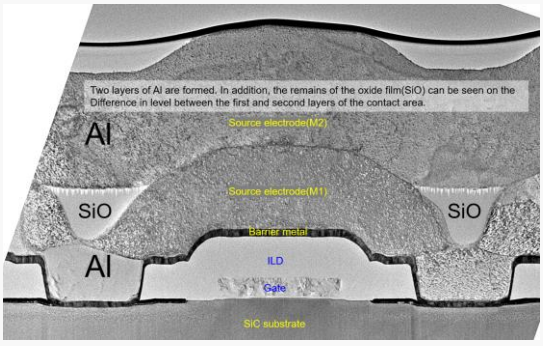
Number	Measurement points		Measurement	Material
1	Mold resin		–	[illegible]
2	Output terminal		–	–
2-1		Plating layer	[illegible]	Sn
2-2		Terminal	[illegible]	Cu
3	Solder		[illegible]	[illegible]
4	Cu ribbon		[illegible]	Cu
5	Solder		[illegible]	[illegible]
6	SiC-MOSFET		–	–
6-1		Protective film	[illegible]	[illegible]
6-2		Top electrode 3	[illegible]	Al/Ni/Ti
6-3		Top electrode 2	[illegible]	[illegible]
6-4		Top electrode 1	[illegible]	[illegible]
6-5		Substrate	[illegible]	SiC
6-6		Back electrode-1	[illegible]	Ti
6-7		Back electrode-2	[illegible]	Ni/V
7	Die attach		[illegible]	Ag
8	DBC substrate		[illegible]	–
8-1		Upper electrode	[illegible]	Cu
8-2		Insulation layer	[illegible]	[illegible]
8-3		Bottom electrode	[illegible]	Cu



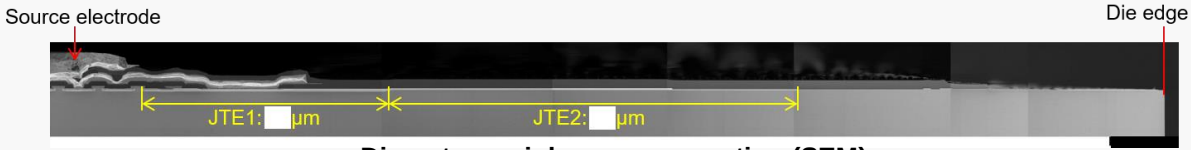
Plane cell array (Poly-Si layer)



Cell array cross-section (SEM)



Cell array cross-section (TEM)



Die outer periphery cross-section (SEM)

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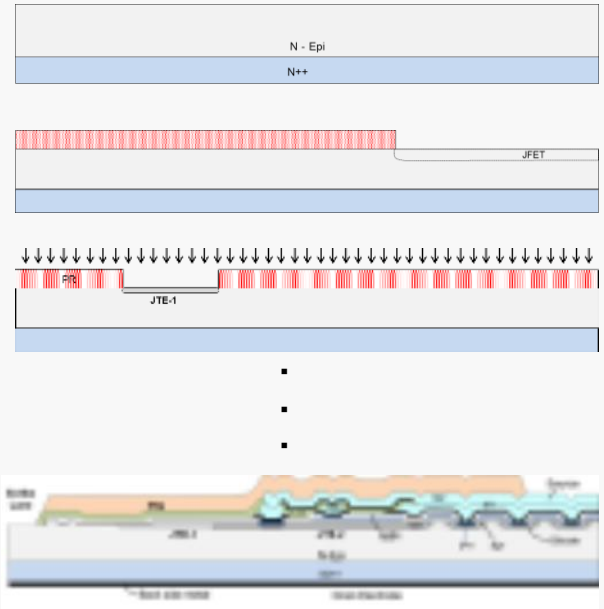
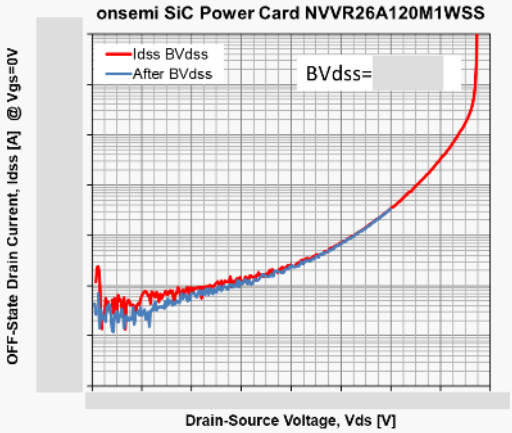
(2) Excerpt from process analysis report

Characteristics comparison between onsemi and other companies' SiC MOSFETs

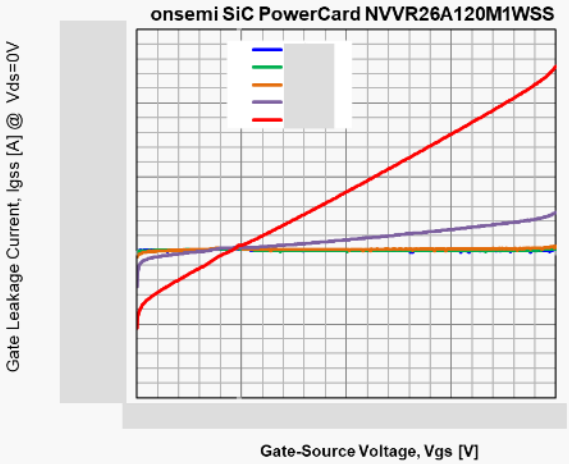
Maker	Part no.	Process generation	Manufacture	Die size mm x mm	mm2	Vdss [V]	RON [mΩ]	Intrinsic RONxA [mΩ·mm^2]
ROHM	SCT3080KL	3rd	2016			1200	80	
ROHM	SCT4062KR	4th	2022			1200	62	
WOLFSPEED	C3M0075120K	3rd	2017			1200	75	
INFINEON	AIMW120R060M1H	1st+	2021			1200	60	
Microsemi	MSC040SMA120B	2nd	2018			1200	40	
GeneSiC	G3R75MT12K	3rd	2020			1200	75	
onsemi	NVHL080N120SC1	1st SC1	2019			1200	80	
onsemi	NVVR26A120M1WSS	M1	2023			1200	15.6	
onsemi	NTH4L022N120M3S	M3S	2022			1200	22	



Process flow (estimate)



Off-state breakdown voltage BVdss



Gate leakage current vs. Gate voltage

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