New Release

# LTEC Corporation

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## SiC MOSFET(1200V)：Infineon IMB120R078M2H Overview, Structure, and Process Analysis Reports


**Package**

**SiC MOSFET**

## Report summary

In January 2024, Infineon announced a new 2nd generation (Gen 2) CoolSiC process technology, 1200V SiC MOSFET (M2H) product (web page). LTEC released the following three analysis reports on this new Gen 2 transistors. (1) Product overvoew reort (2) Structure analysis report, and (3) Process flow analysis report.

The characteristics of the 1200V transistor used in Infineon CoolSiC have evolved in the approximately six years since Gen 1 in 2017 to Gen 2. This report gives insights on Infineon's approach and strategy for the development of advanced SiC MOSFETs.

## Product specifications/features

Product： IMBG120R078M2H 1200V, 29A, 78.1mΩ. Released: January 2024.

## Reports Contents/Overview of Results (Table o Contents P.2, P.4 and P.6)

### 1. Overview analysis report (17 pages)

- Package and die observation, size measurements
- SiC MOSFET cross-sectional analysis: cell part dimensions, epi structure, thicknesses

### 2. Structure analysis Report (72 pages)

- Packaging/mounting technology: Ultra-thin die attach using .XT technology.
- Structural comparison with Gen 1+ CoolSiC (M1H) products: Shrunk transistor cell size.
- TEM observation of gate insulating film.
- Includes the contents of the above Overview analysis report

### 3. Process analysis Report (48 pages)

- Achieves specific on-resistance RONxAA=180mΩ▪mm$^2$, ~18% lower than other companies' 4th generation. RONxAA reduction compared to CoolSiC Gen 1+ M1H technology.
- The channel carrier mobility is 3 to 4 times higher than that of competitors' SiC transistors.
- Low RON temperature dependence inferred to correlate with low SiC/SiO2 interface traps.
- N-epi (drift) impurity concentration profile extraction. Estimated to include redesign and high concentration CSL (current spreading layer).

**Please contact us for report pricing**

LTEC Corporation US Representative Office Phone: (408) 489-1994
No.203 2880 Zanker Road San Jose, CA 95034 www.ltecusa.com Contact: Contact2@ltecusa.com

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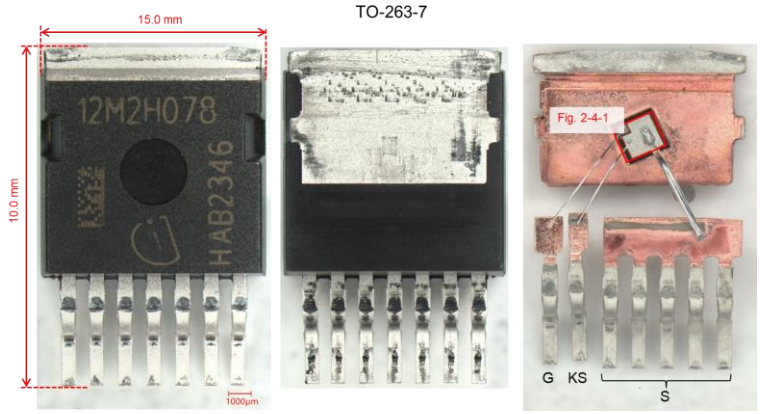
Release day：2024.03.25

# ① Excerpt from Overview analysis report (1)

# ① Excerpt from Overview analysis report (2)

## 2-1. Package appearance




**SiC MOSFET**

## 1-4. Device structure: SiC MOSFET

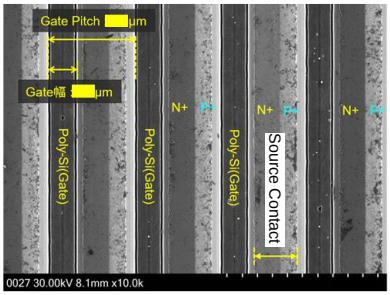



Fig.1-4-1 SiC MOSFET cell array

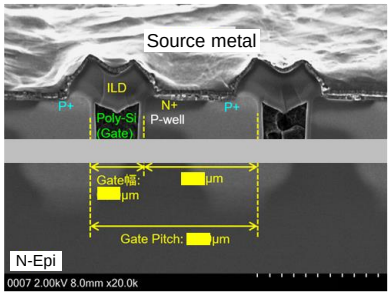



Fig.1-4-2 SiC MOSFET SEM cross-section

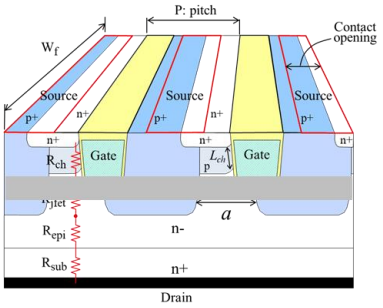
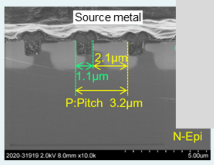
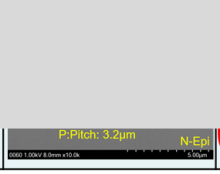



Fig.1-4-3 SiC MOSFET cross sectional schematic

### 4. CoolSiC Gen1 and Gen2 Comparison

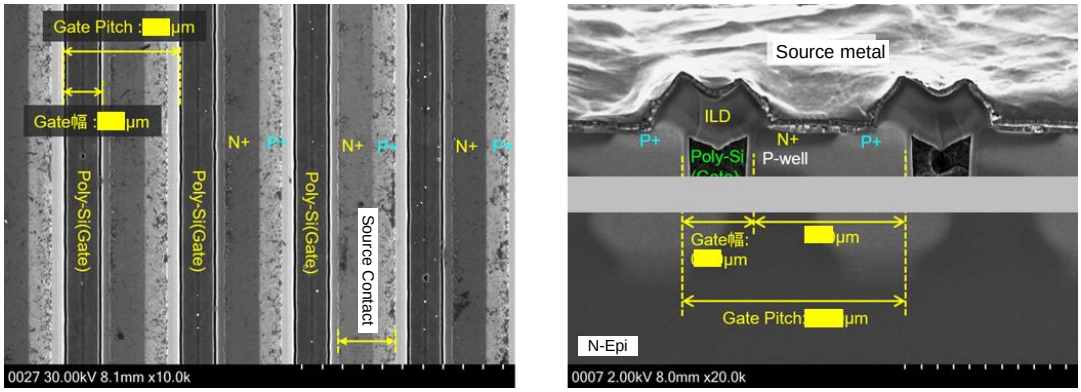
| | | AIMW120R060M1H | AIMBG120R010M1H | IMBG120R078M2H | ROHM SCT34062KR |
|---|---|---|---|---|---|
| Process generation | - | Gen 1 | Gen 1+ | Gen 2 | Gen 4 |
| Min/Max Vgs | V/V | -7/23 | | | 23 |
| ON resistance RON/ Vgs | mΩ / V | 60 / 18 | | | 18 |
| Specific ON resistance RON x AA | mΩ·mm² | 257 | | | 9 |
| RONxAA、relative change | % | 100% | | | 5% |
| Die size | mm x mm | 2.77 x 2.27 | | | 2.65 |
| Transistor Active Area, AA | mm² | 4.29 | | | 54 |
| Cell Pitch, P | μm | 3.2 | | | 0 |
| Cell area cross-sectional SEM image | - |  |  |  | |

# ② Excerpt from Structure analysis report (1)

# ② Excerpt from Structure analysis report (2)

**Table1-3: Device structure : Layers material and thickness**

| Description | Thickness | Material | Properties |
|---|---|---|---|
| Wafer type/configuration (Bulk, Epi) | 109µm | SiC | Crystal Orientation: NE |
| N-epi layer | | | |
| N Buffer layer | | | |
| P diffusion | | | |
| N+ diffusion | | | |
| Gate electrode | | | |
| Gate dielectric | | | |
| Field Oxide | | | |
| Silicide layer | | | |
| Source barrier metal | | | |
| Source metal | | | |
| ILD (Gate-Metal) | | | |
| Passivation layer | | | |
| Protection layer | | | |
| Die backside metal | | | |




Transistor Cell SEM observation

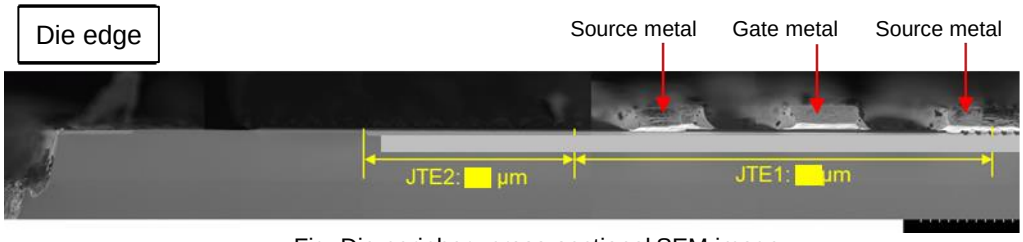



Fig. Die periphery cross-sectional SEM image

# ③ Excerpt from Process analysis report (1)

# ③ Excerpt from Process analysis report (2)

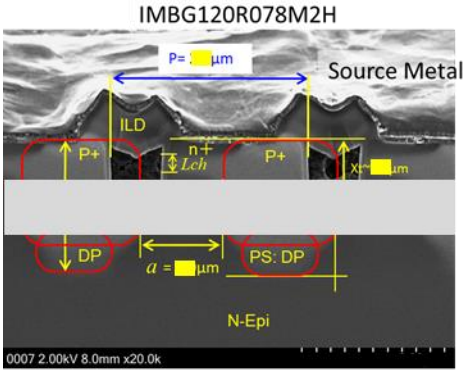



Fig. 1-6-2 Transistor cell

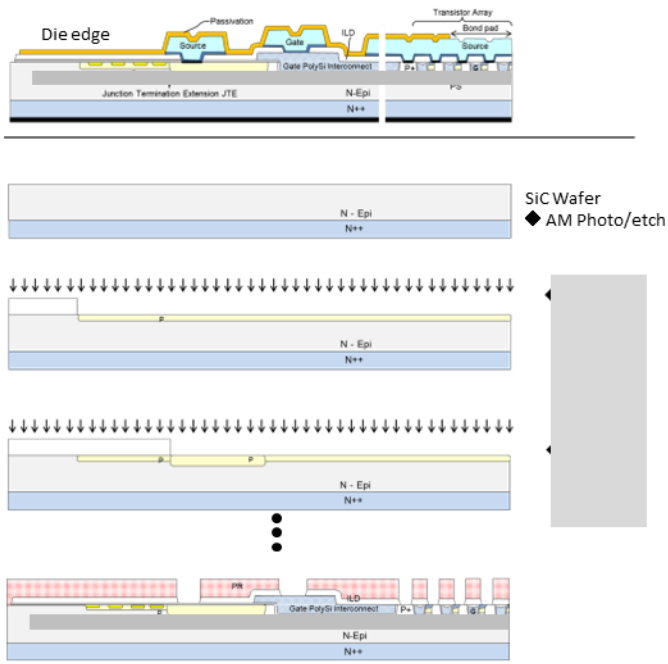
Asymmetric trench gate MOSFET. The P diffusion region is deeper and o… P) regio… he trencl… itial contr… conce… nt is use… T chara… ote that t… be becau… assur… ess.

*The … most … WOL… MOS… one MOS… el effici… differ… region.

Table 5-1: Comparison of evolution and characteristics of CoolSiC MOSFETs

| | | | INFINEON | | | WOLFSPEED | ROHM |
|---|---|---|---|---|---|---|---|
| # | | Units | IMW120R045M1 | AIMBG120R010M1 | IMBG120R078M2H | C3M0075120K | SCT4062KR |
| 1 | Technology production start | | 2017 | 2023 | 2024 | 2017 | 2022 |
| 2 | Technology generation | | Gen 1 | Gen 1+ | Gen 2 | Gen 3 | Gen 4 |
| 3 | Max Drain Voltage, Vdss | V | 1200 | 1200 | 1200 | 1200 | 1200 |
| 4 | Gate-Source transient voltage range, Vgs | V | | | | | 4 ~ 23 |
| 5 | Recommended Vgs (for spec Ron) | V | | | | | 18 |
| 6 | ON Resistance (Typ) @ Tc-25℃ | mΩ | | | | | 62 |
| 7 | Intrinsic specific ON resistance RONxAA | mΩ·mm² | | | | | 219 |
| 8 | Triode β/W | mA/V²mm | | | | | 1.7 |
| 9 | MOSFET Channel Length, Lch ※) | µm | | | | | 0.24 |
| 10 | Gate Dielectric (Oxide) Thickness, Tox | nm | | | | | 50 |
| 11 | MOSFET Channel Effective Mobility, µch | cm²/V·s | | | | | ~6 |
| 12 | Transconductance gm/W (Vds=10V) | mS/mm | | | | | 2.3 |
| 13 | JFET Pinch-off Voltage, Vp | V | 6.2 | 19 | 13 | 10 | 4 |

3-2. Schematics of the SiC MOSFET process sequence



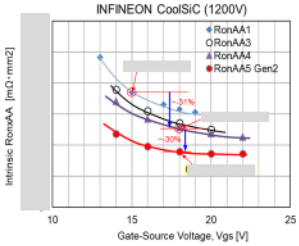




Fig. 5-3: Change in intrinsic per area on-resistance (RonxAA) as a function of gate-source voltage (Vgs) for CoolSiC SiC MOSFETs

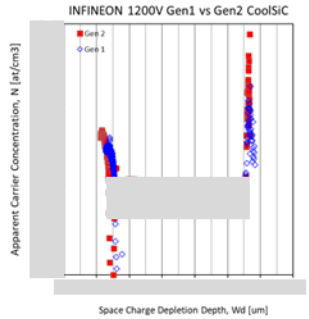



Fig.4-9: (c) Carrier concentration profile in the depth direction