New Release

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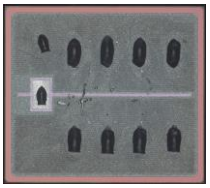
SiC MOSFET(1200V) : WOLFSPEED 4th Gen E4M0013120K Overview, Structure, and Process Analysis Reports

Package



SiC MOSFET

Overview

In June 2024, WOLFSPEED, the world's largest manufacturer of SiC wafers, released their 4th -generation 1200V SiC MOSFET. LTEC released three reports. (1) Die overview analysis, (2) Structural analysis of the die (including a comparison with 3rd-generation products), (3) Manufacturing process and electrical characteristics analysis report.

Product features

＊Contact LTEC for the structural analysis report (23G-0478-1) of the 3rd Generation product.

- Product number : E4M0013120K 1200V, 153A, 13mΩ Released: June 2024.
- Automotive qualified (AEC-Q101) and PPAP compliant
- Applications: Motor Control, EV Battery Chargers, High Voltage DC/DC Converters

Reports Contents/Overview of Results

1. Overview Analysis Report (11 pages)

- Observation of the package and die, and cross-section of the transistor cell and chip end.

2. Structure analysis Report (78 pages)

- The 4th Gen die size is 17% smaller than the 3rd Gen product having same Ron=13mΩ.
- As new feature, the transistor cell array (planar) of this product has a honeycomb structure.
- The contents of the 1. Overview analysis report are also included.

3. Process analysis Report (47 pages)

- The specific on-resistance (RonxAA) is compared with MOSFETs from major manufacturers (ROHM, INFINEON).
- The Ron components are quantitatively analyzed, and the effect of the new structure and layout (honeycomb) in reducing RonxAA and channel resistance component Rch is revealed.
- The manufacturing process and photo/mask are estimated, and comprehensive details of the manufacturing sequence are shown.
- The evolution of WOLFSPEED's technology and improvements from the 2nd to 4th generations are surveyed, and the company's development strategy can be inferred.

Please contact LTEC for delivery time and prices for optional SCM analysis.

Report price

Delivered one week after order placement **Please contact us for report pricing.**

LTEC Corporation US Representative Office www.ltec-biz.com/en/
2310 Homestead Rd, C1 #231 Los Altos, CA 94024
Phone: +1-(650) 382-1181
Contact2@ltec.biz

Report No : 24G-0327-2, 24R-0327-1,3
Release day : 2024.08.20

(1) Overview Analysis Report:

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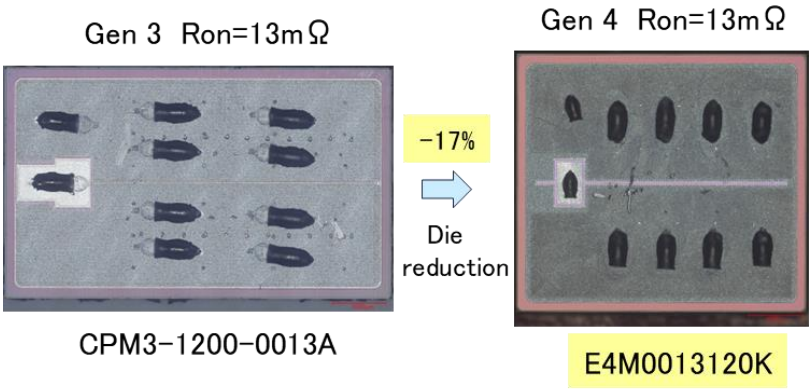
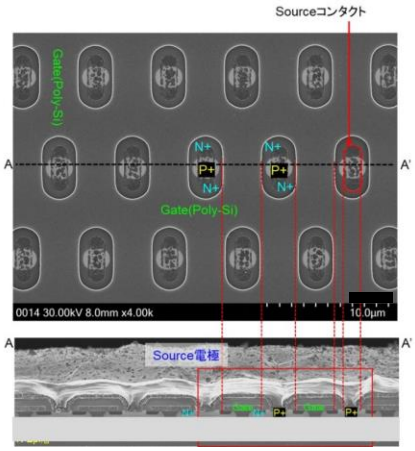
Excerpt from (1) Overview Analysis Report



Comparison of WOLFSPEED's 3rd and 4th generation SiC chips



Planar and cross-sectional SEM images of cell array

Table1-3: Device structure:SiC MOSFET

Die size	mm x mm		
Die area, A	mm^2		
Transistor Active Area, AA	mm^2		
Transistor array configuration	Ho		
Basic structure of a transistor cell (Gate)			
Cell Source-Source Pitch, P	μm		

Table1-4: Device structure: Layers' materials and thicknesses

Description	Thickness	Material	Remarks
Wafer type (Bulk, Epi)			
N-epi			
Gate electrode structure and materials			
Gate dielectric			
Silicide			
Source barrier metal	1		
ILD (Gate-Metal)			
Passivation layer			

(2) Structural Analysis Report

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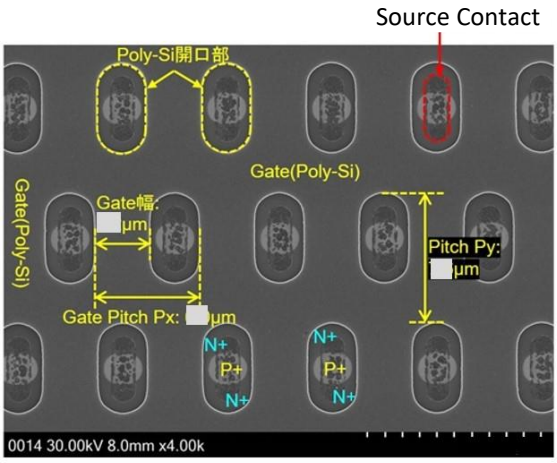
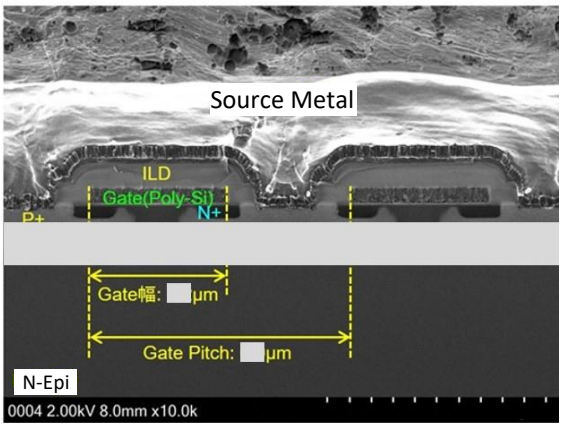
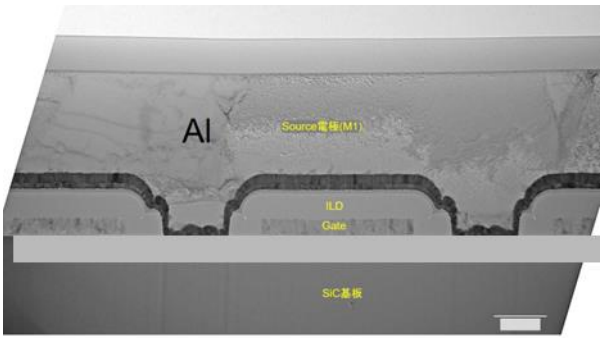
Excerpt from (2) Structure Analysis Report



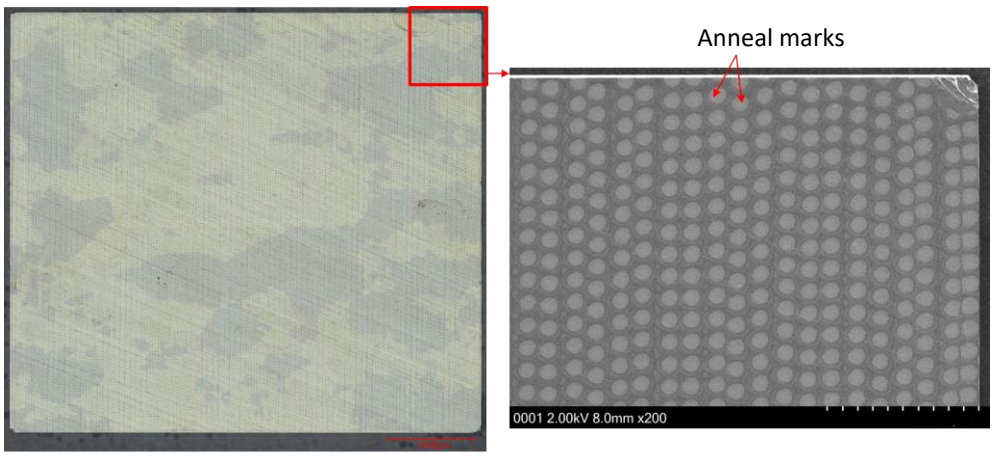
Cell array: Planar SEM image (Poly-Si layer)



Cell array: cross-sectional SEM image



Cell array: cross-sectional TEM image



OM image of the backside of SiC MOSFET die

LTEC Corporation US Representative Office www.ltec-biz.com/en/
2310 Homestead Rd, C1 #231 Los Altos, CA 94024
Phone: +1-(650) 382-1181
Contact2@ltec.biz

(3) Process Analysis Report

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Excerpt from (3) Process Analysis Report

Transistor structure and process features (3)

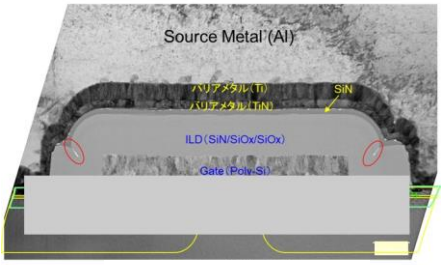
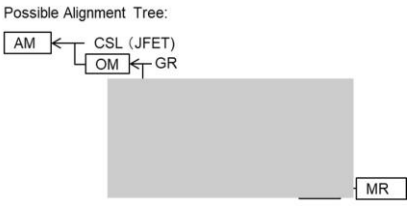


Fig.2-1-5 Transistor array TEM image



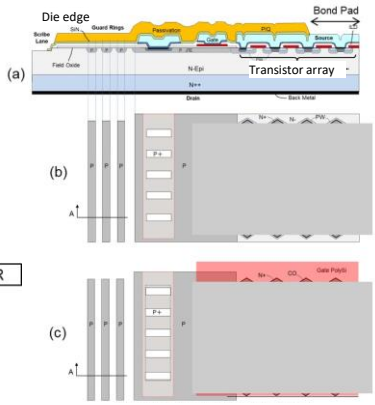
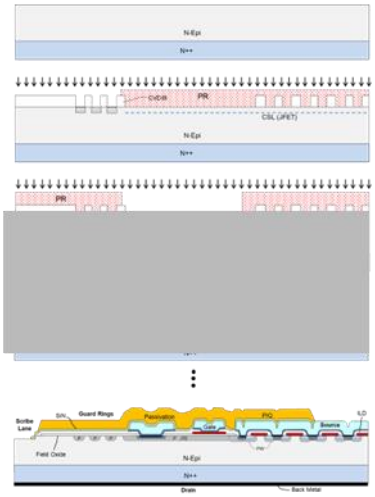


Fig.4-2-1 Transistor cross-section and layout schematics

WOLFSPEED SiC MOSFET E4M0013120K Process flow sequence



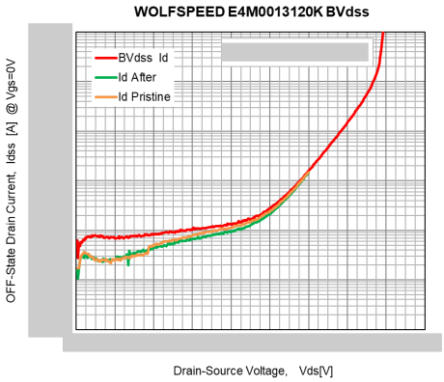


Fig.5-5-1 OFF-state breakdown voltage BVdss

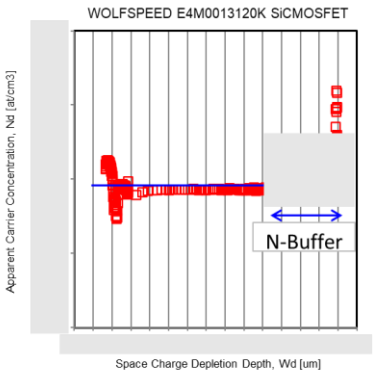


Fig.5-9-1(a) Carrier doping profile in depth direction

Table 6.1 Evolution of WOLFSPEED technology and improvements from 2nd to 4th generation

Product name		C2M0080120D	C3M0075120K	EA8450M12XM3 (Module) CPM3-1200-0013A (Chip)	E4M0013120K
SiC MOSFET Technology Gen. /生産開始		2nd /~2013年	3rd/ 2016年	3rd/ 2022-23年	4th/ 2024年
Package		TO-247	TO-247-4L	Module and Bare die	TO-247-4L
Transistor Size	mm x				
Transistor Area, A	mm				
Transistor Active Area, AA	mm				
Total Channel Width, W	mm				
Layout Efficiency, W/AA	mm/				
Rated Vdss	V				
Measured Breakdown Voltage, BVdss	V				
DC Id @ Tc=25°C	A				
Tjmax	°C				
Operating Gate Source voltage	V				
RON @ T=25°C	mΩ				
Specific ON resistance, RONxAA	mΩ•c				
Threshold Voltage, Vth	V				
Transconductance, gm @Vds=20V	A/				
Transistor configuration (N+/Pwell)					onal
Gate dielectric thickness, Tox	nn				
Triode transconductance parameter, β	A/V				
Normalized mobility: (β/W)•(1/Cox)					
MOSFET Channel Resistance, Rch/RON	%				
Process changes from previous generation					

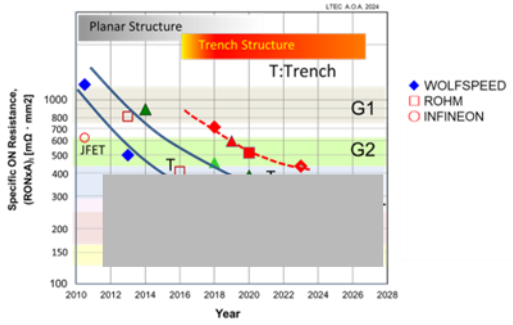


Fig.6-2-1 Trend in the specific ON resistance index (RONxA) of 1200V SiC MOSFETs