New Release

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SiC MOSFET(1200V): Inventchip Gen3 IV3Q12013T4Z Overview, Structure, Process and Electrical characteristics Analysis Reports

Package

Inventchip Gen3 SiC MOSFET die

Overview

Inventchip, a major Chinese SiC manufacturer, announced Gen1 SiC MOSFETs in 2019(*), Gen2 SiC MOSFETs in 2023, and Gen3 SiC MOSFETs in June 2024.

This Gen3 SiC MOSFET is a product that shows the progress of China's SiC technology, as it is the same RonxA as the major SiC manufacturers (Infineon, Wolfspeed, Rohm, STMicroelectronics).

In order to clarify the features of this product, we released the following three reports (1) Overview (2) Structure analysis (3) Process and electrical characteristic analysis.

(*)The Gen1 analysis report 21G-0033-3 is now on sale.

Product features

- Product type: IV3Q12013T4Z V_{DS}= 1200V I_D= 147A $R_{DS(on)}$ = 13.5 mΩ
- Released: June 2024
- Automotive qualified (AEC-Q101)、 Applications: EV Motor drivers、Solar MPPT and inverters

Report Contents/Overview of Results

(1) Overview Analysis Report (13 pages)

- Package observation, die observation, size measurement
- Cross-section: Die edge, cell array (Checking epi structure and film thickness)

(2) Structure Analysis Report (84 pages)

- Includes the contents of (1) the overview analysis report, TEM structure analysis of the cell array, and analysis of annealing marks on the backside of the die.
- We have revealed that there are concerns about the reliability of this product.

(3) Process and Electrical characteristics Analysis report (36 pages)

- The manufacturing process and photo/mask are estimated, and the manufacturing sequence details are shown.
- Comparison of RonxAA with the Gen1 and major manufacturers (It is comparable to STMicro' Gen3.)

Report price

Delivered one week after order placement **Please contact us for report pricing.**

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Report No :24R-0641-1,2,3
Release day:2024.11.29

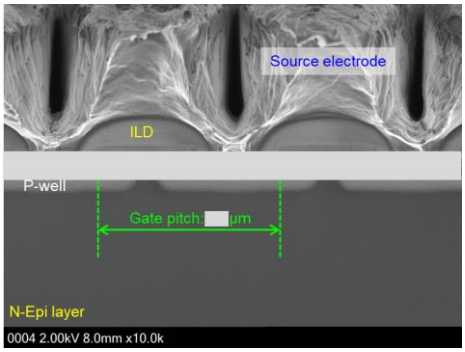
(1) Overview Analysis Report table of contents

Excerpt from (1) Overview Analysis Report

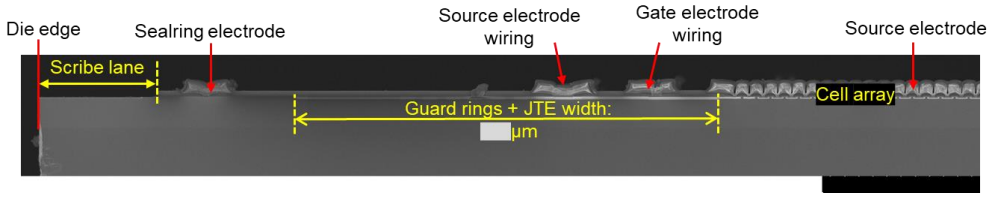
Table1-1： Device summary

Device	SiC MOSFET (VDSS=1200V, $R_{DS(ON)}$(Typ.) = 13.5mΩ (V_{GS} = 18V), I_D = 147A)
Manufacturer	Inventchip Technology Co., Ltd. (China)
Product name	IV3Q12013T4Z
Package type	TO-247-4
Package marking	3Q12013T4Z 2425S HA3H
Die configuration	Transistor: SiC MOSFET x1
Die size	5.0 mm x 5.0 mm = 25.0 mm²
SiC MOSFET Die manufacturing process	SiC wafer, planer gate, top metal source
Feature	• [redacted]
Application	• EV Motor drivers • Solar MPPT and inverters • High Voltage DC/DC Converters • Switch mode power supplies

Device summary



Cross-sectional SEM image of cell array



Cross-sectional SEM image of die outer periphery

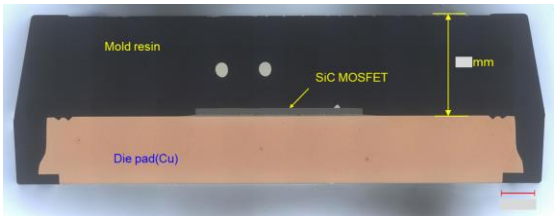
Table4-1: Comparison

		IV1Q12080T3 (Gen1)	IV3Q12013T4Z (Gen3)	Wolfspeed E4M0013120K (Gen4)
ON resistance: RON	(mΩ) / Vgs (V)	80 / 20	13.5 / 18	13 / 15
ON resistance per unit area RONxAA	mΩ·mm²	[redacted]	[redacted]	[redacted]
Die size	mm x mm = mm²	[redacted]	[redacted]	[redacted]
Transistor active area AA	mm²	[redacted]	[redacted]	[redacted]

Comparison with Gen1 product and the major manufacturers products

(2) Structure Analysis Report table of contents

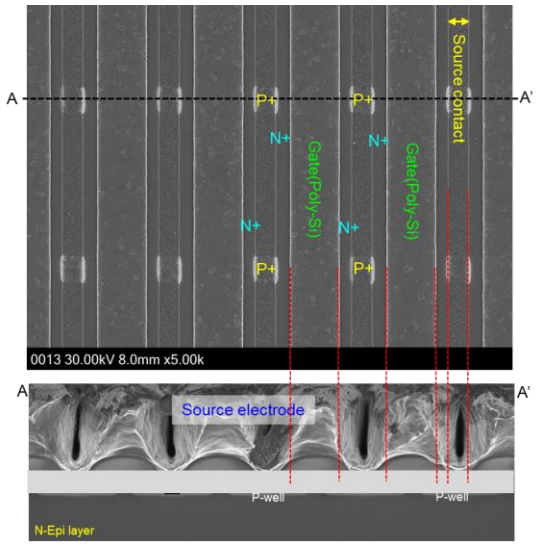
Excerpt from (2) Structure Analysis Report



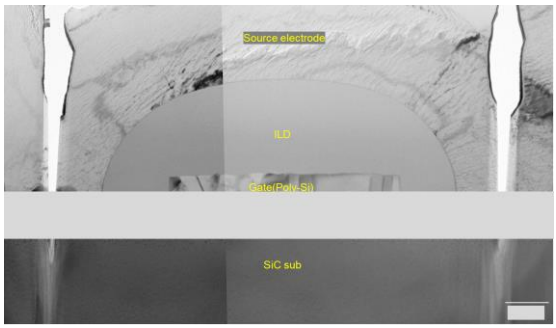
Package cross-sectional structure

番号	測定箇所		測長	材料
1	Mold resin			
2	Al wire			
2-1		Wire diameter : Gate		
2-2		Wire diameter : Source		
2-3		Wire average length		
3	SiC-MOSFET			
3-1		Surface protection film		
3-2		Top metal		
3-3		Substrate		
3-4		Backside metal-1		
3-5		Backside metal-2		
3-6		Backside metal-3		
4	Die attach			
5	Die pad			
5-1		Die pad		
5-2		Plating layer		

Package cross-sectional structure summary



Alignment of cell plane structure and cross-sectional structure



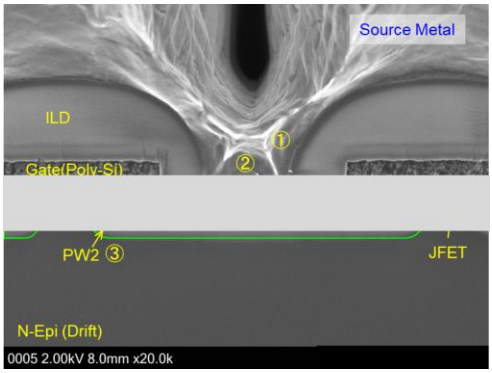
Cross-sectional TEM image of cell array

	IV1Q12080T3 (Gen1)	IV2Q12040T4Z (Gen2)	IV3Q12013T4Z (Gen3)
Epi layer thickness (μm)			
Cell pitch (μm)			
ILD shape			
P-well implantation depth (μm)			

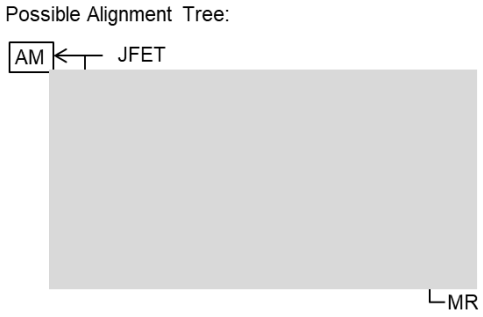
Comparison with previous generation products (Cell cross-sectional structure)

(3) Process and Electrical characteristics Analysis Report table of contents

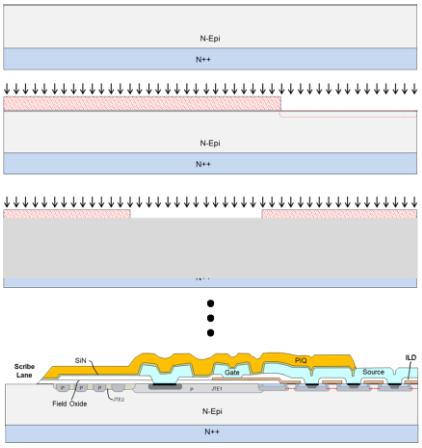
Excerpt from (3) Process and Electrical characteristics Analysis Report



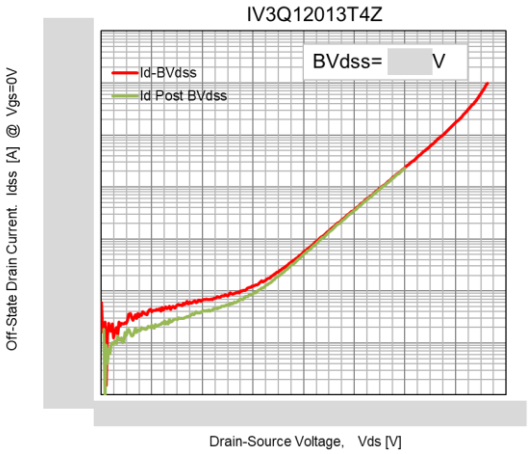
Transistor cell



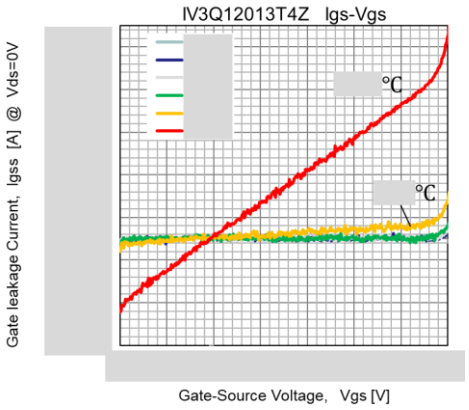
Alignment Tree



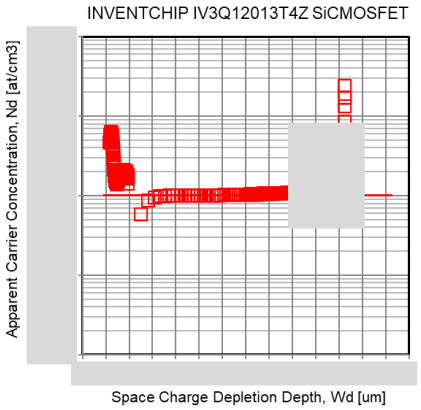
SiC MOSFET process sequence (estimated)



Off-state breakdown voltage BVdss



Gate leakage current vs. Gate-Source voltage



Carrier concentration profile in the depth direction

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