



LTEC Corporation

Your most experienced partner in IP protection

SiC MOSFET(1200V) : Coherent TM3B0020120A Structure Analysis Report





Overview

Coherent, Inc. in America (formerly Π -VI) is a global SiC wafer manufacturer that competes with Wolfspeed and SiCrystal. Coherent manufactures and sells discrete SiC MOSFET products under a license from General Electric (GE). This report is a structure analysis report on the cell structure and the outer peripheral structure of the SiC MOSFET released by Coherent.

Product features

- Product no : TM3B0020120A V_{DSS} =1200V, I_D=115A, R_{DS(ON)}=20m Ω Product release date: April 2024
- 200°C rated

Report Contents (77 pages)

- GE's dot-type JTE structure is designed to reduce the area compared to other manufacturers' technology while relaxing electric field concentration at the cell edge and maximizing the transistor area. (The related patents for the JTE structure are listed in the report.) JTE: Junction Termination Extension
- Polycide is formed to reduce the resistance of the gate electrode (Poly-Si).
- Based on the cell pitch and RonAA, it is believed that SiC process technology equivalent to third generation or higher is being used.

Report price

Delivered one week after order placement. Please contact us for report pricing.

We are also planning to provide a process analysis report and detailed package material analysis report for this product. If you are interested, please contact LTEC.



LTEC Corporation US Representative Office www.ltec-biz.com/en/ 2310 Homestead Rd, C1 #231 Los Altos, CA 94024 Phone: +1-(650) 382-1181 contact2@ltec.biz

Report No : 23G-0838-1 Release day : 2024.06.24

Exe	cerpt from Structure analysis report (1)		
-			
	ABLE OF CONTENTS		Page
1	Device summary		
	Table1-1: Device summary	•••	3
	1-1. Summary of analysis results	•••	4
	Table1-2: Device structure : SiC MOSFET	•••	5
	Table1-3: Device structure: Layer material and thickness	•••	6
	Table1-4: Device structure : Package structure overview	• • •	7
2	Package analysis		
	2-1. Appearance observation	•••	9
	2-2. Mounted die observation	•••	12
	2-3. Package cross-sectional structure analysis	• • •	13
3	SiC MOSFET die structure analysis		
	3-1. Plane structure analysis by Optical Microscope	•••	27
	3-2. Plane structure analysis by SEM	• • •	40
	3-3. Cross-sectional structure analysis of cell area	• • •	48
	3-4. Cross-sectional structure analysis of die outer periphery	•••	56
	3-5. Cross-sectional structure analysis of Gate electrode pad	•••	62
4	Cross-sectional TEM structure analysis		66
5	SiC MOSFET die backside structure analysis (Analysis of annealing marks)	•••	72
6	Appendix: About JTE structure	•••	75



LTEC Corporation US Representative Office www.ltec-biz.com/en/ 2310 Homestead Rd, C1 #231 Los Altos, CA 94024 Phone: +1-(650) 382-1181 contact2@ltec.biz

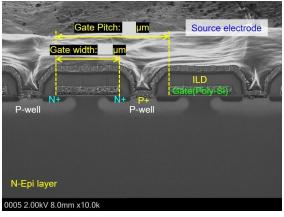
Excerpt from Structure analysis report (2)



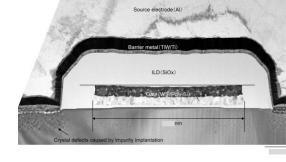
Package cross-sectional structure

Number	Measure points		ure points	Measurement	Material
1	Mold resin			-	
2	Al wire				
2-1			Gate		
2-2	1		Source		
3	SIC-MOSFET				
3-1	Organic protective film		protective film		
3-2	Top metal		tal		
3-3	Substrate		te		
3-4	Backside metal-1		le metal-1		
	Backside metal-2 Backside metal-3 Die attach Die pad		le metal-2		
3-5			le metal-3		
4					
5			757		
5-1			Die pad		
5-2	1		Plating		

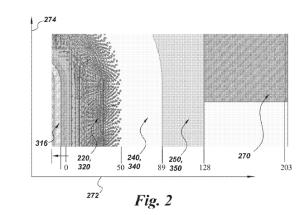
Package cross-sectional structure overview



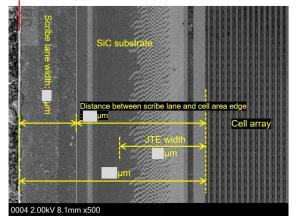
Cross-sectional SEM image of cell area



Cross-sectional TEM image of cell area



Drawing (Related patents of JTE structure)



Plane SEM image of die outer periphery

TP Service

LTEC Corporation US Representative Office www.ltec-biz.com/en/ 2310 Homestead Rd, C1 #231 Los Altos, CA 94024 Phone: +1-(650) 382-1181 contact2@ltec.biz

Die edge