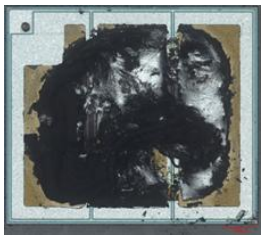
Si MOSFET(150V) : iDEAL Semiconductor SuperQ MOSFET (Super Junction) iS15M7R1S1C Structure Analysis Report

Package



Si MOSFET die

Report Overview

iDEAL Semiconductor, a fabless semiconductor manufacturer based in Lehigh Valley, Pennsylvania, has begun mass production of a family of products called SuperQ Power MOSFETs. This SuperQ Power MOSFET technology is derived from an SJ-MOS-like resurf structure, and uses proprietary trench isolation technology and doping concentrations to rival wide bandgap semiconductors in key performance areas such as RonAA and blocking voltage.

This time, LTEC released a structure analysis report that clarifies structure features of this product through plane and cross-section analysis.

Product Features

Product type : iS15M7R1S1C V_{DS}=150V、I_D=133A、$R_{DS(ON)}$=5.4mΩ

Released data: June 2025

Datasheet：https://idealsemi.com/wp-content/datasheets/iS15M7R1S1C-Datasheet.pdf

・Applications: AI data centers, high voltage DC power conversion, etc.

Analysis result summary

Structure Analysis Report (75 pages)

The transistor cells of this product are Si SJ MOSFETs with a trench gate structure, with an ALD (Atomic Layer Deposition) layer formed on the sidewalls of the trench. In terms of performance, when compared to the Infineon 150V SiMOSFET (OptiMOS 5) with a similar rating to this product, the RonxAA of this product is about 2/3 of that of OptiMOS 5.

(*) A separate SCM analysis is required to confirm the ALD layer.Please contact us for more details. We can also create manufacturing process sequence and electrical characteristic analysis reports for this product. If you are interested, please contact us.

Report price

Delivery within 1 week after ordering. Please contact us for prices.

Report No. 25R-0332-1 Released data: 2025.10.17

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(※)Related patent: US20240145532A1

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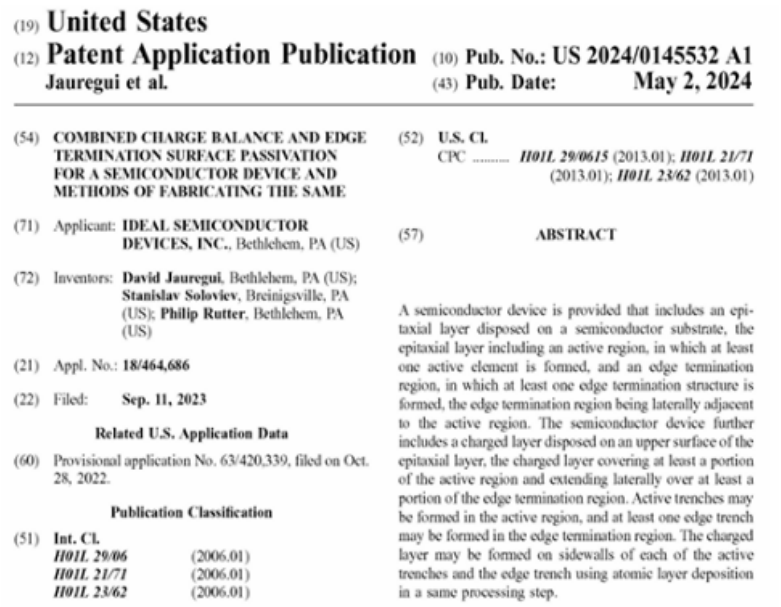
Excerpt from Structure Analysis Report

Tc = 25℃		Infineon OptiMOS 5 IPB060N15N5	iDEAL Semi SuperQ iS15M7R1S1C
Vdss	(V)	150	150
Transistor active area AA	(mm^2)		
Ron	(mΩ / Vgs(V))		
Ron x AA	(mΩ · mm^2)	90	60
Cell pitch P	(μm)		
Cell structure features			Gate (Poly-Si) trench, ALD trench (ALD layer doping (P type) on trench sidewall)

Comparison with Infineon's 150V Si MOSFET (OptiMOS 5)



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Jauregui et al. (43) **Pub. Date: May 2, 2024**

(54) **COMBINED CHARGE BALANCE AND EDGE TERMINATION SURFACE PASSIVATION FOR A SEMICONDUCTOR DEVICE AND METHODS OF FABRICATING THE SAME**

(71) Applicant: **IDEAL SEMICONDUCTOR DEVICES, INC.**, Bethlehem, PA (US)

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(21) Appl. No.: **18/464,686**

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Related U.S. Application Data

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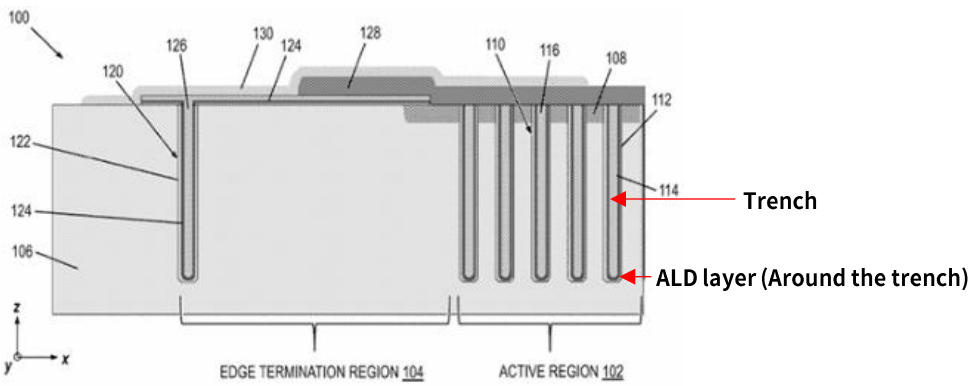
(57) **ABSTRACT**

A semiconductor device is provided that includes an epitaxial layer disposed on a semiconductor substrate, the epitaxial layer including an active region, in which at least one active element is formed, and an edge termination region, in which at least one edge termination structure is formed, the edge termination region being laterally adjacent to the active region. The semiconductor device further includes a charged layer disposed on an upper surface of the epitaxial layer, the charged layer covering at least a portion of the active region and extending laterally over at least a portion of the edge termination region. Active trenches may be formed in the active region, and at least one edge trench may be formed in the edge termination region. The charged layer may be formed on sidewalls of each of the active trenches and the edge trench using atomic layer deposition in a same processing step.

Related Patent Overview (US20240145532A1)



Related patent drawings (US20240145532A1)

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