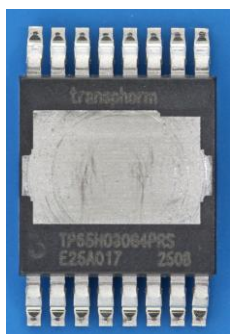
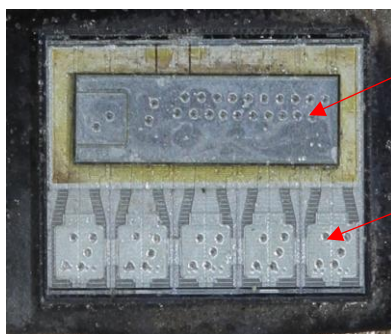


GaN FET (650V): Renesas Electronics TP65H030G4PRS Package and GaN FET structure analysis report



Package



GaN FET + Si MOSFET die

Si MOFET

GaN FET

Report Overview

Renesas Electronics has launched and begun mass production of a new 650V high-voltage gallium nitride (GaN) power semiconductor.

The new product adopts a new process called “4th Generation Plus (Gen IV Plus).” Compared to the conventional 4th Generation (Gen IV), it achieves improved power efficiency by reducing the die size by 14% and lowering the on-resistance to 30 mΩ. The product also features the proven SuperGaN technology* of Transphorm, a company acquired in June 2024.

The product is suitable for 1kW to 10kW power supply systems such as AI servers, EV charging systems, UPS (uninterruptible power supplies), and solar power inverters.

LTEC released reports on the package structure analysis of this product and the GaN FET die structure analysis equipped in it.

SuperGaN : A normally-off GaN FET utilizing a cascode structure that connects a high-voltage D-mode GaN and a low-voltage Si MOSFET in series.

Product Features

Product type: TP65H030G4PRS $V_{DS}=650V$, $I_D=55.7A$, $R_{DS(ON)}=30m\Omega$

Released data: June 2025

[Product Information TP65H030G4PRS](#)

FOM : Qgd • Ron= 198 nC • mΩ (Si SuperJunction : 740~868 nC • mΩ)

Analysis result summary

1. Package Structure Analysis Report (34 pages)

Analysis of materials such as bonding wires and die attach was conducted, along with measurements of the film thickness of each layer. Si MOSFET is vertically stacked on the GaN FET die, and it also conducted observation and analysis of the connection materials between Si MOSFET and GaN FET die.

2. GaN FET Structure Analysis Report (90 pages)

Metal layout of each layer, thickness of each metal layer and GaN epi layer, and material analysis of GaN FET dies. In particular, this analysis revealed that passive elements not listed in the equivalent circuit on the datasheet are formed on GaN FET die.

Report price

Delivered one week after order placement. Please contact us for report pricing.

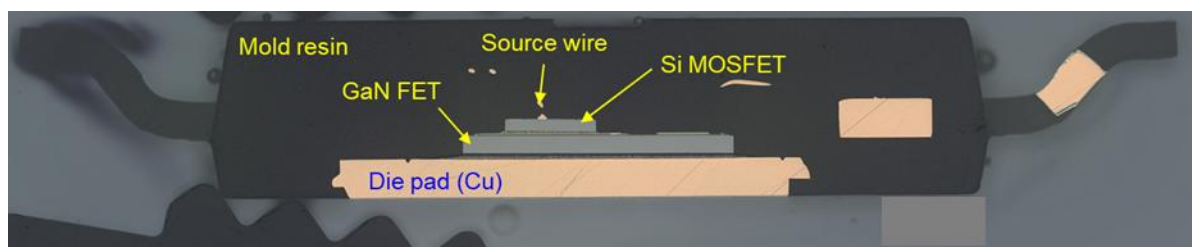
① Package Structure Analysis Report Table of Contents

【Table of Contents】			Page
1	Device Summary		
	Table 1: Device Summary	• • •	3
1-1	Summary of analysis results	• • •	4
2	Package analysis		
2-1	Appearance	• • •	7
2-2	Internal layout observation	• • •	9
2-3	Die Observation	• • •	10
2-4	Package Cross Section Structure Analysis	• • •	10
2-5	Lead frame dimensions	• • •	32

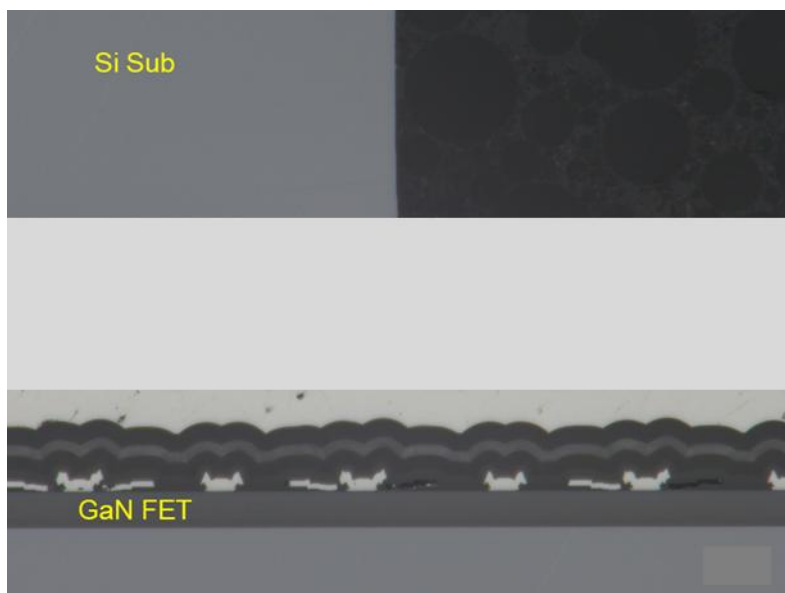
2. GaN FET Structure Analysis Report Table of Contents

【Table of Contents】			Page
1	Device Summary		
	Table 1: Device Summary	• • •	3
1-1.	Summary of Analysis Results	• • •	4
	Table.1-1-1:Device Structure (GaN FET)	• • •	5
	Table.1-1-2:Device Structure: Layer Materials and Film Thickness (GaN FET))	• • •	6
1-2.	Die Configuration Summary	• • •	7
2	Plane Structure Analysis	• • •	12
2-1.	Plane OM Structure Analysis	• • •	13
2-2.	Plane SEM Structure Analysis	• • •	35
3	Cross Section SEM Structure Analysis	• • •	41
4	Cross Section TEM Structure Analysis	• • •	65
5	TEM-EDX Analysis	• • •	75
6	Appendix	• • •	88

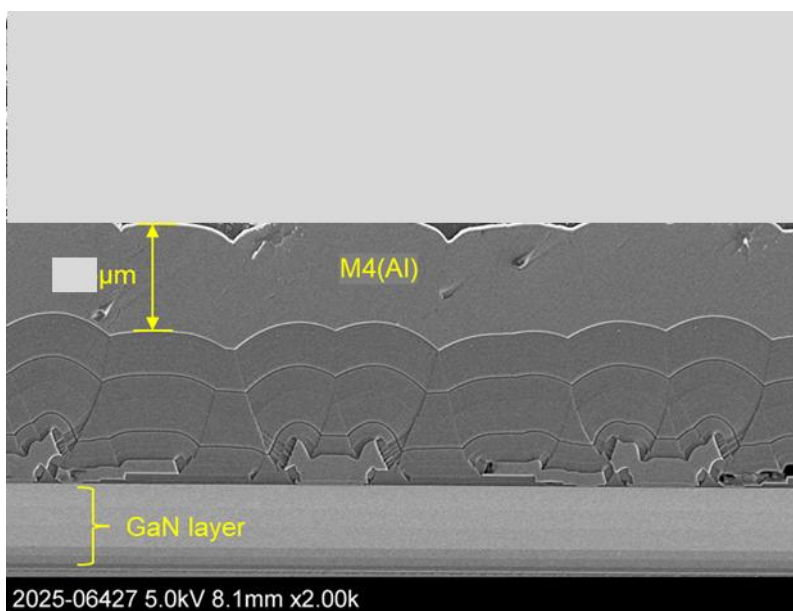
① Excerpt from Package Analysis Report



Package Cross-Section Structure

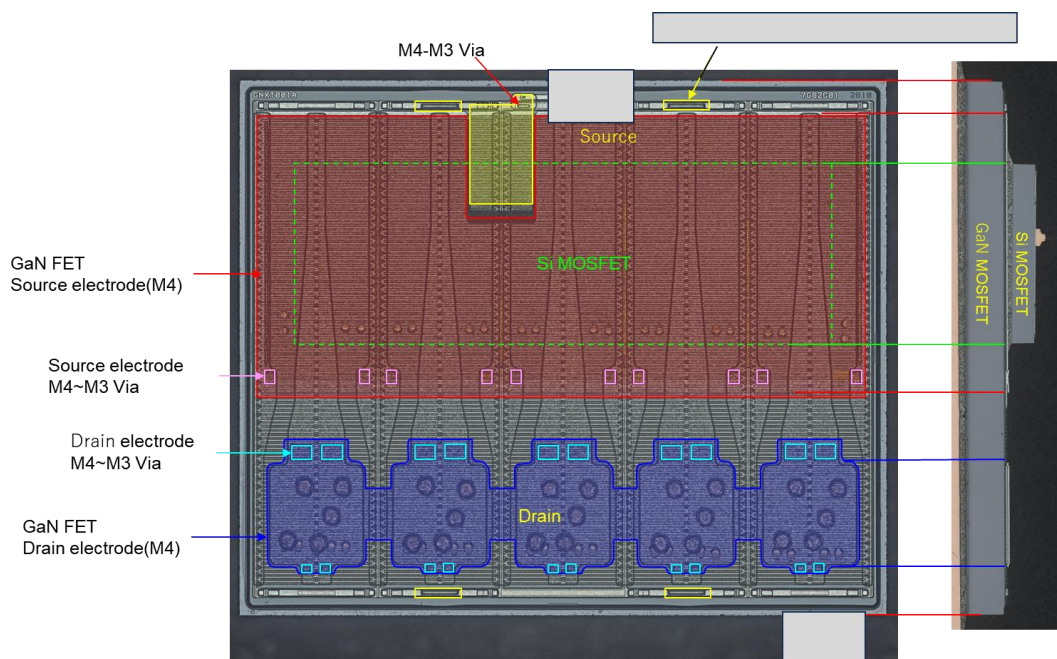


Si MOSFET-GaN FET Connection Cross-Section

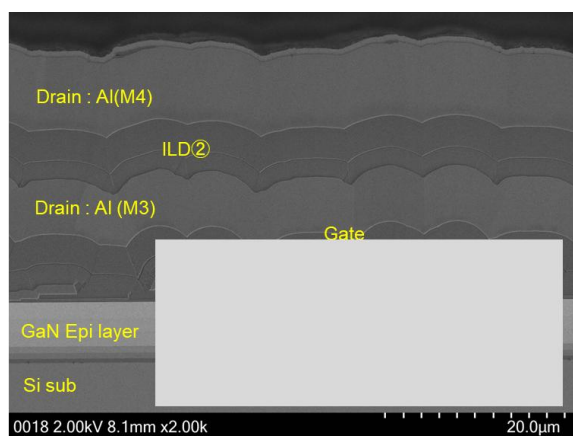


Si MOSFET-GaN FET Connection Cross-Section

② Excerpt from GaN FET Structure Analysis Report

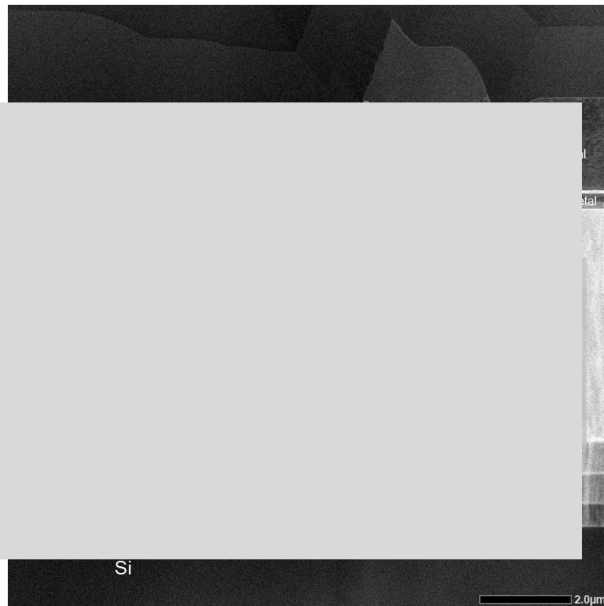


Die layout (Top metal layer)



Cell array cross-section SEM image

Dark Field image



Cell array cross-section TEM image (GaN-Epi layer)