

## SiC MOSFET(1200V) : Nomis Power N3T080MP120D Overview Analysis Report



Package



SiC MOSFET die

### Report Overview

Nomis Power was founded in 2020 as a spin-out from the University at Albany in the United States, and in 2024 the company released its first lineup of 1200V SiC MOSFET products.

N3T080MP120D is one of the products in this lineup, and in this analysis report, it conduct a simplified analysis of the die structure and transistor cell cross-section of N3T080MP120D to clarify the technical characteristics of Nomis Power's products, along with a comparison to products from other manufacturers.

In addition, Nomis Power highlights the high reliability of the gate oxide as a key feature of this product. To verify this, LTEC are also planning structure analysis reports focusing on (1) the thickness of the gate oxide layer and (2) the strength of the gate oxide ( $I_{GSS}$ —

### Product Features

Product type: N3T080MP120D  $V_{DS}=1200V$ 、 $I_D=38A$ 、 $R_{DS(ON)}=80m\Omega$  Released data: Aug. 2024

Datasheet : <https://nomispower.com/wp-content/uploads/2024/08/NoMIS-Power-N3T080MP120D.pdf>

Applications: EV on-board chargers, EV fast charging stations, motor drives, solar PV inverters, etc.

### Analysis result summary

#### Overview Analysis Report (15 pages)

- This product's specific resistance  $R_{on} \times A$  (active area) is  $321 \text{ m}\Omega/\text{mm}^2$ , which, according to LTEC's database, corresponds to third-generation technology.
- A hexagonal planar gate structure is used.
- As the edge termination structure, two types of guard rings and a JTE (Junction Termination Extension) are employed, and the width of the peripheral region is more than twice that of other products with the same voltage rating.

If you are interested in the detailed structure analysis report or the short-circuit withstand evaluation report of this product, please contact us.

### Report price

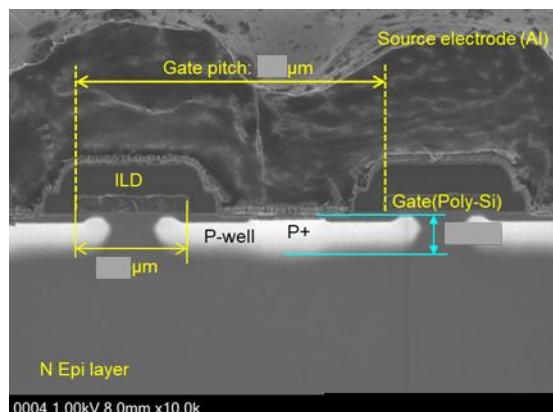
Delivered one week after order placement. Please contact us for report pricing.

[Table of Contents]	Page
1 Device Summary	• • • 3
Table 1: Device Summary	• • • 3
1-1. Summary of Analysis Results	• • • 4
Table1-2: Device structure: SiC MOSFET	• • • 4
Table1-3: Device Structure: Layer Materials and Film Thickness	• • • 5
2 Package observation	
2-1. Appearance observation	• • • 7
3 SiC MOSFET die Overview Analysis	
3-1. Plane Overview Analysis (OM) (Die Observation)	• • • 9
3-2. Cell array Cross-section Analysis (Epi Film thickness and Cell pitch)	• • • 10
3-3. Die Periphery Cross-section Analysis (Breakdown Voltage Structure)	• • • 11
3-3. Outer Peripheral cross-section overview Analysis	• • • 11
4 Comparison with Other Manufacturers	• • • 12-15

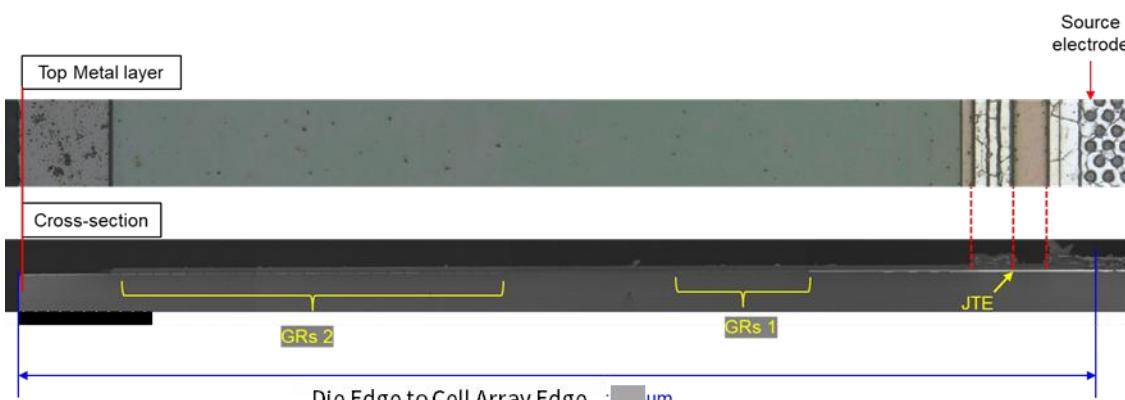
## Excerpt from Overview Analysis Report



SiC MOSFET (Top metal layer)



Cell array cross-section SEM Image



Die Periphery cross-section SEM Image